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Docket No.
ITL.1059US

In Representation Of: Ramesh V. Peri, et al.

Application No. 10/717,085	Filing Date November 19, 2003	Examiner Paul W. Schlie	Customer No. 21906	Group Art Unit 2186	Confirmation No. 7032
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Invention: Accessing Data from Different Memory Locations in the Same Cycle

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June 9, 2006

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Dated: July 11, 2006

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Applicant:

Ramesh V. Peri

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Art Unit: 2186

Serial No.: 10/717,085

Examiner: Paul W. Schlie

Filed: November 19, 2003

Atty Docket: ITL.1059US
(P17918)

For: Accessing Data from Different
Memory Locations in the Same Cycle

Assignee: Intel Corporation

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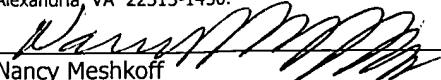

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TABLE OF CONTENTS

REAL PARTY IN INTEREST.....	3
RELATED APPEALS AND INTERFERENCES.....	4
STATUS OF CLAIMS	5
STATUS OF AMENDMENTS	6
SUMMARY OF CLAIMED SUBJECT MATTER	7
GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL	11
ARGUMENT	12
CLAIMS APPENDIX.....	13
EVIDENCE APPENDIX.....	17
RELATED PROCEEDINGS APPENDIX	18

REAL PARTY IN INTEREST

The real party in interest is the assignee Intel Corporation.

RELATED APPEALS AND INTERFERENCES

None.

STATUS OF CLAIMS

Claims 1-28 (Rejected).

Claims 1-28 are rejected and are the subject of this Appeal Brief.

STATUS OF AMENDMENTS

All amendments have been entered.

SUMMARY OF CLAIMED SUBJECT MATTER

In the following discussion, the independent claims are read on one of many possible embodiments without limiting the claims:

1. A method comprising:
implementing read accesses to the same portion of a memory line in the same cycle (Figure 3, block 48, specification at page 4, line 24 to page 5, line 10).

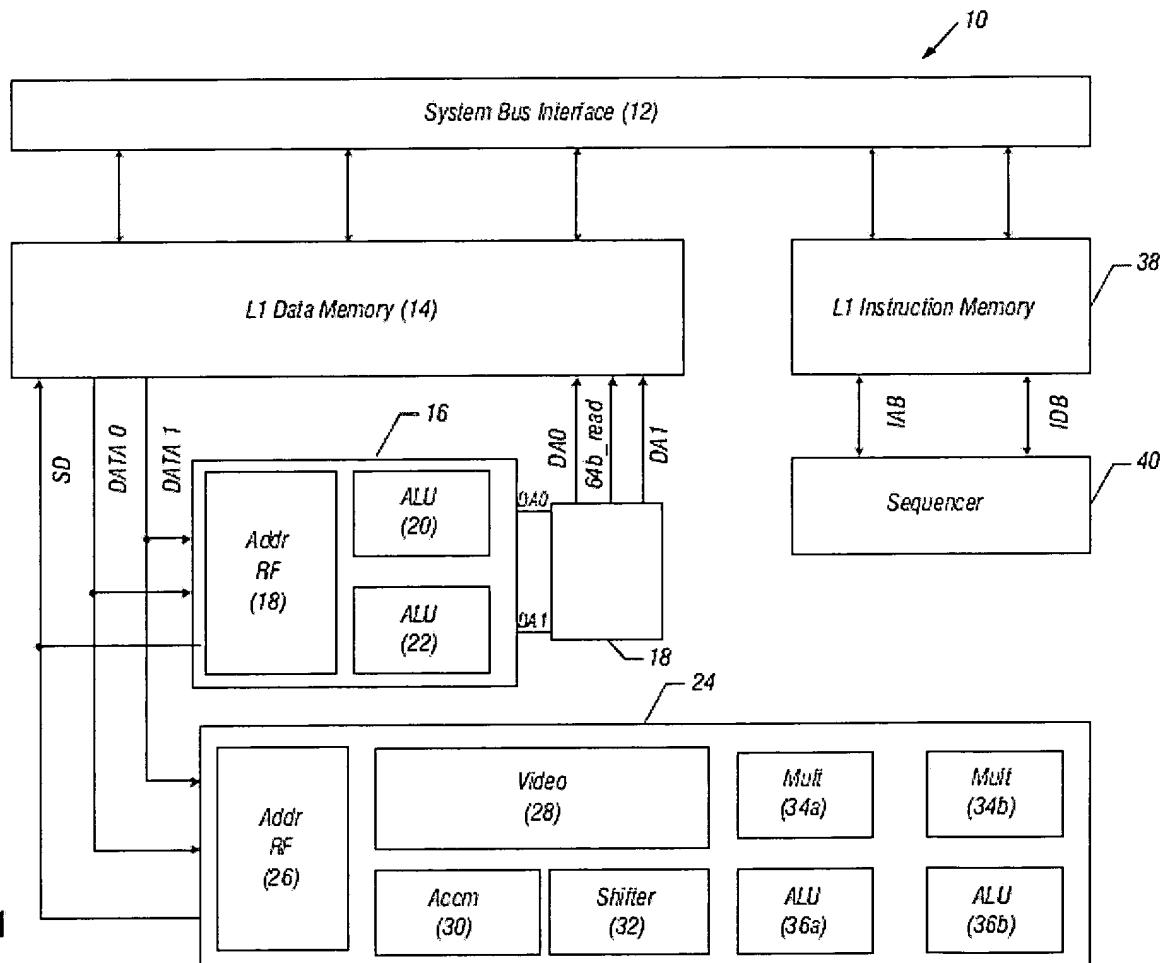


FIG. 1

9. An article comprising a medium storing instructions that, if executed, enable a processor-based system to:

determine whether two read accesses are to the same portion of a memory line (Figure 3, diamond 46, specification at page 4, lines 3-10); and

if so, implement the read accesses from the portion in the same cycle (Figure 3, block 48, specification at page 4, line 24 to page 5, line 10).

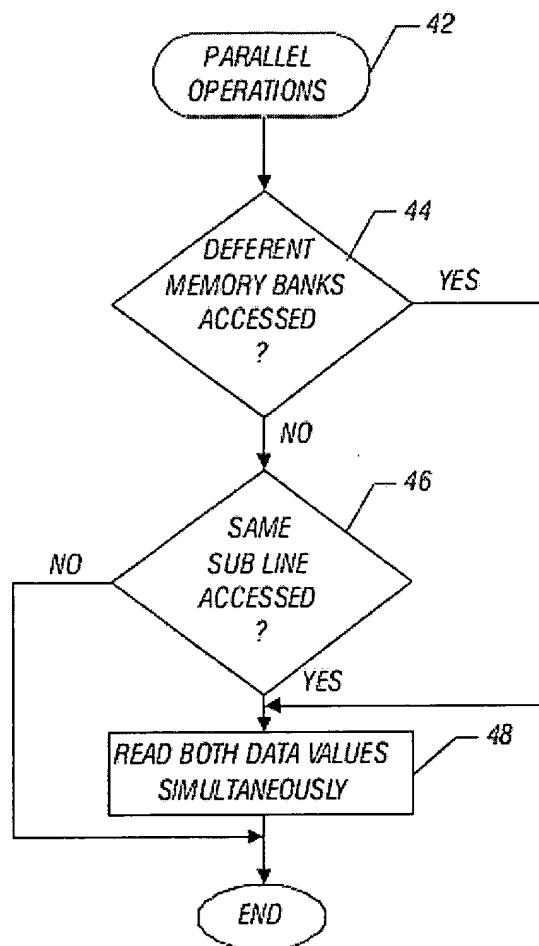


FIG. 3

15. A processor comprising:
 a data memory (Figure 2, 14, specification at page 2, lines 13-20); and
 a controller (Figure 2, 18, specification at page 3, line 12 to page 4, line 13) to access said data memory, said controller to implement read accesses to the same portion of a memory line in the same cycle.

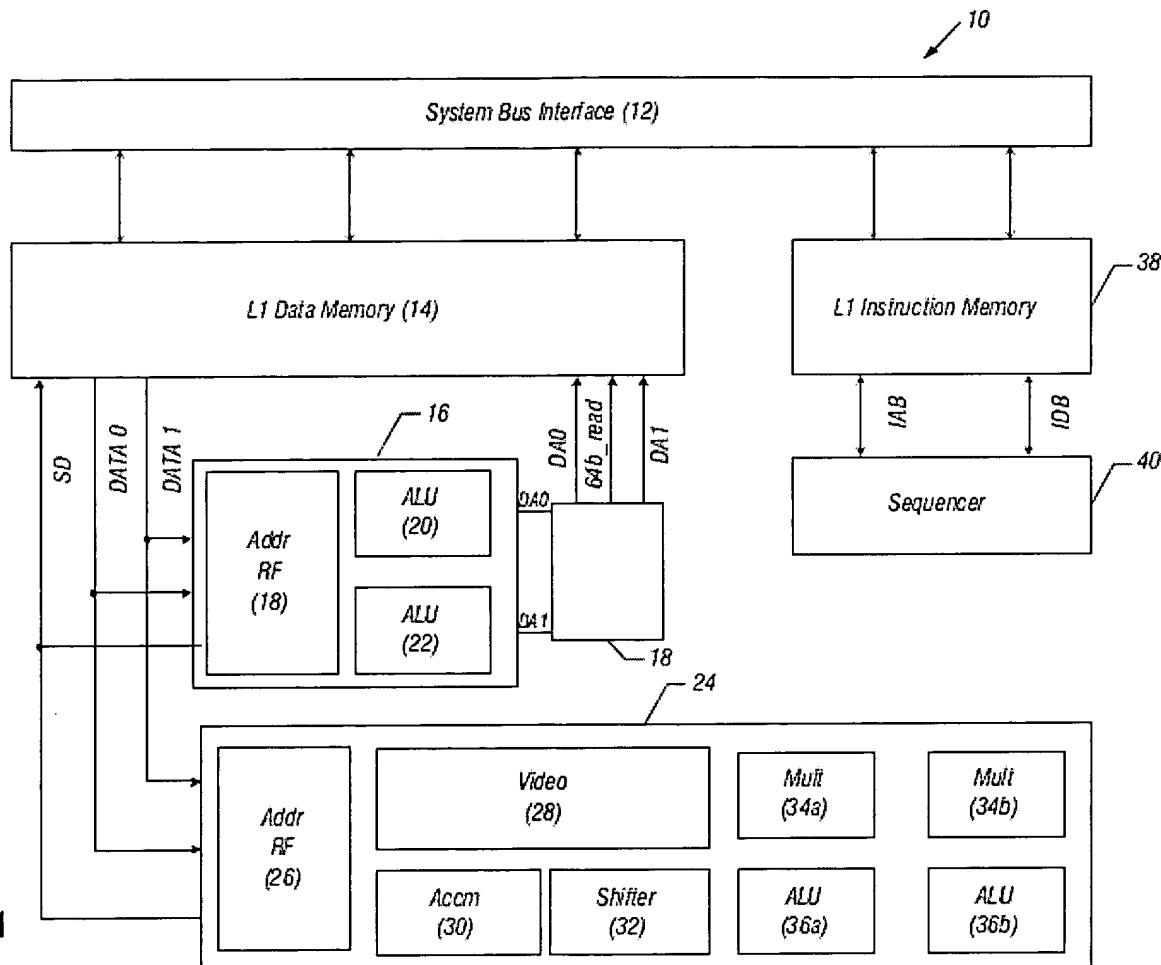


FIG. 1

23. A system comprising:
a digital signal processor (Figure 4, 10);
a general purpose processor (Figure 4, 52);
a bus (Figure 4, 54) coupled to said digital signal processor and said general purpose processor; and

 said digital signal processor including a data memory (Figure 2, 14) and a controller Figure 2, 8) to access the data memory, said controller to determine whether two read accesses are to the same portion of a memory line and, if so, implement the read accesses from the same portion in the same cycle (Figure 3, 46, 48, specification at page 4, lines 3-10 and 24 to page 5, line 10).

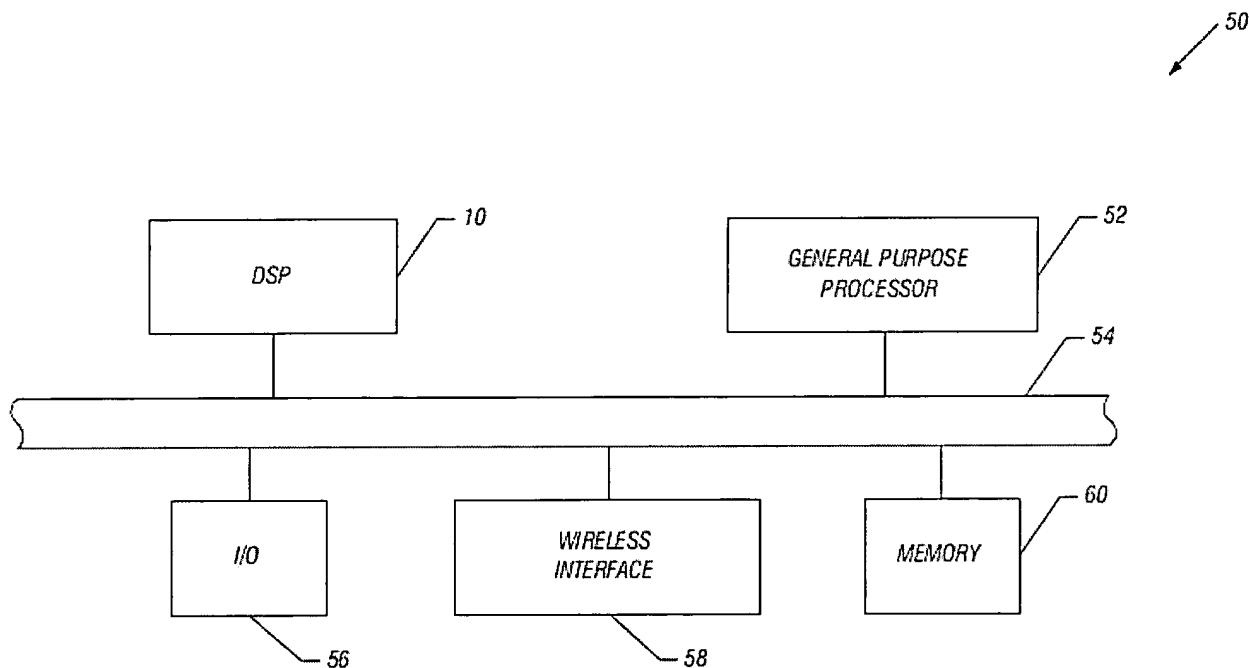


FIG. 4

At this point, no issue has been raised that would suggest that the words in the claims have any meaning other than their ordinary meanings. Nothing in this section should be taken as an indication that any claim term has a meaning other than its ordinary meaning.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Are claims 1-28 anticipated by or obvious over Kawasaki?

ARGUMENT

A. Are claims 1-28 anticipated by or obvious over Kawasaki?

Claim 1 calls for implementing read accesses to the same portion of a memory line in the same cycle.

The final rejection asserts that simultaneous writes to the same address “inherently require logical sequential prioritization to deterministically resolve the logical conflict being introduced in such an event.” Certainly, the argument is not commensurate with the claims since the claim has nothing to do with writes. Since no reference teaches simultaneous writes and no claim covers simultaneous writes, the argument seems to be both irrelevant and improper.

It is not seen how simultaneous writes to the same address would even be possible, much less inherent in the cited reference. Further explanation would be required to establish inherency because, most certainly, nothing in the reference teaches true simultaneous operation of any type, much less simultaneous writes. To be inherent, something must necessarily happen.

Non-simultaneous reads and non-simultaneous writes are both possible and more probable. The suggestion that all simultaneous reads and writes are considered obvious design choices is not defensible. Simultaneous writes to the same address are not claimed, but, certainly if they were claimed, they would not be an obvious design choice.

Applicant respectfully requests that each of the final rejections be reversed and that the claims subject to this Appeal be allowed to issue.

Respectfully submitted,

Date: July 11, 2006



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CLAIMS APPENDIX

The claims on appeal are:

1. A method comprising:
implementing read accesses to the same portion of a memory line in the same cycle.
2. The method of claim 1 including determining whether two read accesses are to the same portion of a memory line by determining whether the read accesses are to the same subline.
3. The method of claim 1 including using a modified Harvard architecture.
4. The method of claim 2 including providing a first portion of the subline on a first bus and a second portion of the subline on a second bus.
5. The method of claim 2 including determining that the read accesses are to the same half of a subline and providing that same half on two different output lines.
6. The method of claim 1 wherein determining includes comparing the addresses of two read accesses to determine whether those read accesses access the same subline.
7. The method of claim 6 including generating a read signal if those read accesses access the same subline.
8. The method of claim 7 including determining whether a 64 bit read has been enabled and, if so, accessing two different portions of the same subline in the same read cycle.

9. An article comprising a medium storing instructions that, if executed, enable a processor-based system to:

determine whether two read accesses are to the same portion of a memory line;
and

if so, implement the read accesses from the portion in the same cycle.

10. The article of claim 9 further storing instructions that enable the processor-based system to determine whether the read accesses are to the same subline.

11. The article of claim 10 further storing instructions that enable a processor-based system to provide a first portion of the subline on a first bus and a second portion of the subline on a second bus.

12. The article of claim 10 further storing instructions that enable the processor-based system to determine that the read accesses are to the same half of a subline and provide that same half on two different output lines.

13. The article of claim 9 further storing instructions that enable the processor-based system to compare addresses to determine whether the read accesses access the same subline.

14. The article of claim 13 further storing instructions that enable the processor-based system to determine whether a 64 bit read has been enabled and, if so, access two different portions of the same subline in the same read cycle.

15. A processor comprising:
a data memory; and
a controller to access said data memory, said controller to implement read accesses to the same portion of a memory line in the same cycle.

16. The processor of claim 15 wherein said controller determines whether the read accesses are to the same subline.

17. The processor of claim 15 wherein said processor uses a modified Harvard architecture.

18. The processor of claim 16 wherein said controller to provide a first portion of the subline on a first bus and a second portion of the subline on a second bus.

19. The processor of claim 16 wherein said controller to determine that the read accesses are to the same half of a subline and provide that same half on two different output lines.

20. The processor of claim 15 wherein said controller to compare the addresses of two read accesses to determine whether said read accesses access the same subline.

21. The processor of claim 20 wherein said controller determines whether a 64 bit read has been enabled and, if so, accesses two different portions of the same subline in the same read cycle.

22. The processor of claim 20 wherein said controller includes a comparator coupled to an AND gate in turn coupled to said data memory.

23. A system comprising:
a digital signal processor;
a general purpose processor;
a bus coupled to said digital signal processor and said general purpose processor;
and

 said digital signal processor including a data memory and a controller to access the data memory, said controller to determine whether two read accesses are to the same portion of a memory line and, if so, implement the read accesses from the same portion in the same cycle.

24. The system of claim 23 wherein said controller determines whether the read accesses are to the same subline.

25. The system of claim 24 wherein said digital signal processor uses a modified Harvard architecture.

26. The system of claim 24 wherein said controller to provide a first portion of said subline on a first bus and a second portion of said subline on a second bus.

27. The system of claim 24 wherein said controller to determine that the read accesses are to the same half subline and provide that same half on two different output lines.

28. The system of claim 24 wherein said controller to compare the addresses of two read accesses to determine whether said read accesses access the same subline.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.